WHAT IS CLAIMED IS:

1. A memory device comprising:

a plurality of pipeline stages for accessing data;

a plurality of clock domains, each clock domain having circuitry controlled by a separate clock;

a clock control circuit configured to selectively supply clock signals to the clock domains so that the clock domains are all activated in advance of, and corresponding to, when the clock domains are needed for a corresponding pipeline stage, all of the clock domains being activated sufficiently in advance so that a clock domain turn-on latency is transparent to a data access.

2. The memory device of claim 1 wherein the clock domains comprise:

a control circuit clock domain; and

a data path stage clock domain.

3. The memory device of claim 1 wherein the stages comprise:

a RAS control stage connected to a first clock domain; and

a CAS control stage connected to a second clock domain.

4. The memory device of claim 1,

a clock source, having at least two clock speeds, for providing clock signals to the plurality of clock domains;

a clock controller configured to dynamically select a clock speed output by the clock source in accordance with a needed bandwidth of the interface.

5. The memory device of claim 4 wherein one of the at least two clock speeds is a slow clock selected by the clock controller when needed bandwidth is determined by the clock controller to be below a predefined threshold, and the slow clock speed is slower than another one of the at least two clock speeds.

6. The memory device of claim 4 wherein the at least two clock speeds includes a first clock speed and a second clock speed that is slower than the first clock speed, the clock controller monitors bus traffic on a memory bus and selects the first clock

speed when bus traffic on the memory bus exceeds a predefined threshold, and selects the second clock speed when bus traffic on the memory bus falls below the predefined threshold.

7. A memory device comprising:

a plurality of pipeline control stages for accessing data;

a plurality of clock domains, each clock domain being connected to one of the stages;

a clock control circuit configured to selectively supply clock signals to the clock domains so that activation of one control stage automatically initiates activation of a subsequent control stage.

8. The memory device of claim 7 wherein a first clock domain includes a sense control circuit, the first clock domain automatically activating a second clock domain including transfer and close control circuits.

9. The memory device of claim 8 wherein a first clock domain includes a transfer write control circuit, the first clock domain automatically activating a second clock domain including a retire write control circuit.

10. A memory device comprising:

a plurality of pipeline control stages for accessing data;

a plurality of clock domains, each clock domain being connected to one of the stages;

a clock control circuit configured to selectively supply clock signals to the clock domains so that activation of one control stage automatically initiates deactivation of a control stage not needed for a subsequent operation.

11. The memory device of claim 10 wherein a first clock domain includes a close operation control circuit, the first clock domain automatically deactivating a second clock domain including transfer and retire write control circuits.

12. A memory system comprising:

a memory;

a memory interface;

at least a portion of one of the memory and the memory interface having at least two clock speeds;

a clock controller configured to dynamically select a clock speed in accordance with a needed bandwidth of the interface.

13. The memory system of claim 12 wherein the clock controller comprises a programmed microprocessor.

14. The memory system of claim 12 wherein one of the at least two clock speeds is a slow clock selected by the clock controller when needed bandwidth is determined by the clock controller to be below a predefined threshold; and the slow clock speed is slower than another one of the at least two clock speeds.

15. The memory system of claim 12 wherein the at least two clock speeds includes a first clock speed and a second clock speed that is slower than the first clock speed, the clock controller monitors bus traffic on a memory bus and selects the first clock speed when bus traffic on the memory bus exceeds a predefined threshold, and selects the second clock speed when bus traffic on the memory bus falls below the predefined threshold.